LOW LATENCY INDUSTRIAL COMMUNICATION BY ORCA SDR

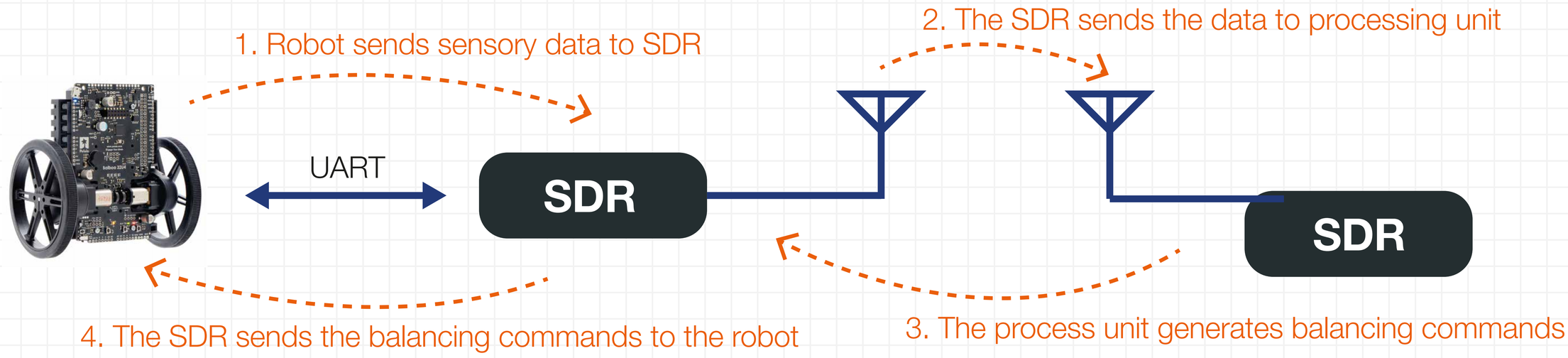
Orchestration and Reconfiguration Control Architecture

ORCA LOW LATENCY SDR SOLUTION

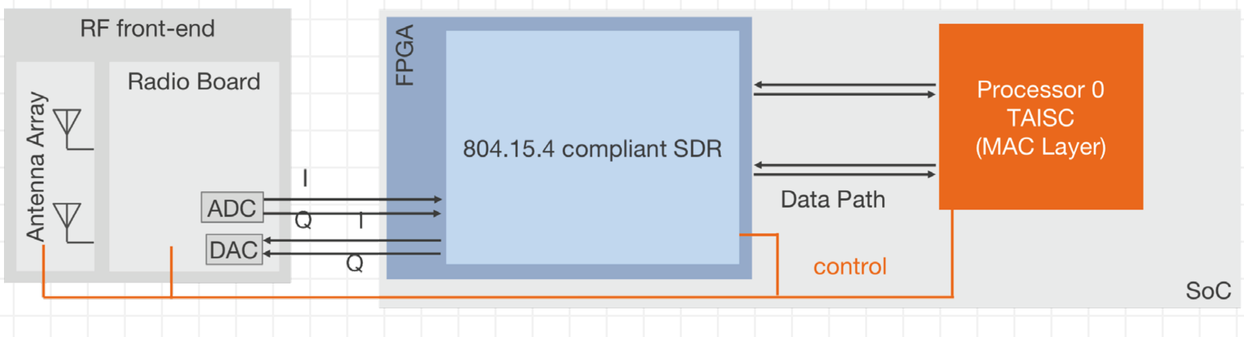
- Tight integration of PHY and MAC
- Offloading functionality to FPGA
- MAC as close to PHY as possible
- Modular PHY/MAC design
- 5G and SDR PHY/MAC latency improvements
- Parameterized reconfiguration of the PHY and MAC

WHY LOW LATENCY SDR SOLUTIONS?

- Ultra reliable low latency communication key for new industrial applications
- Improved reliability/control of SDR networks (PHY or MAC improvements)



SDR SOLUTION 1: LOW COST FLEXIBLE IOT PHY/MAC



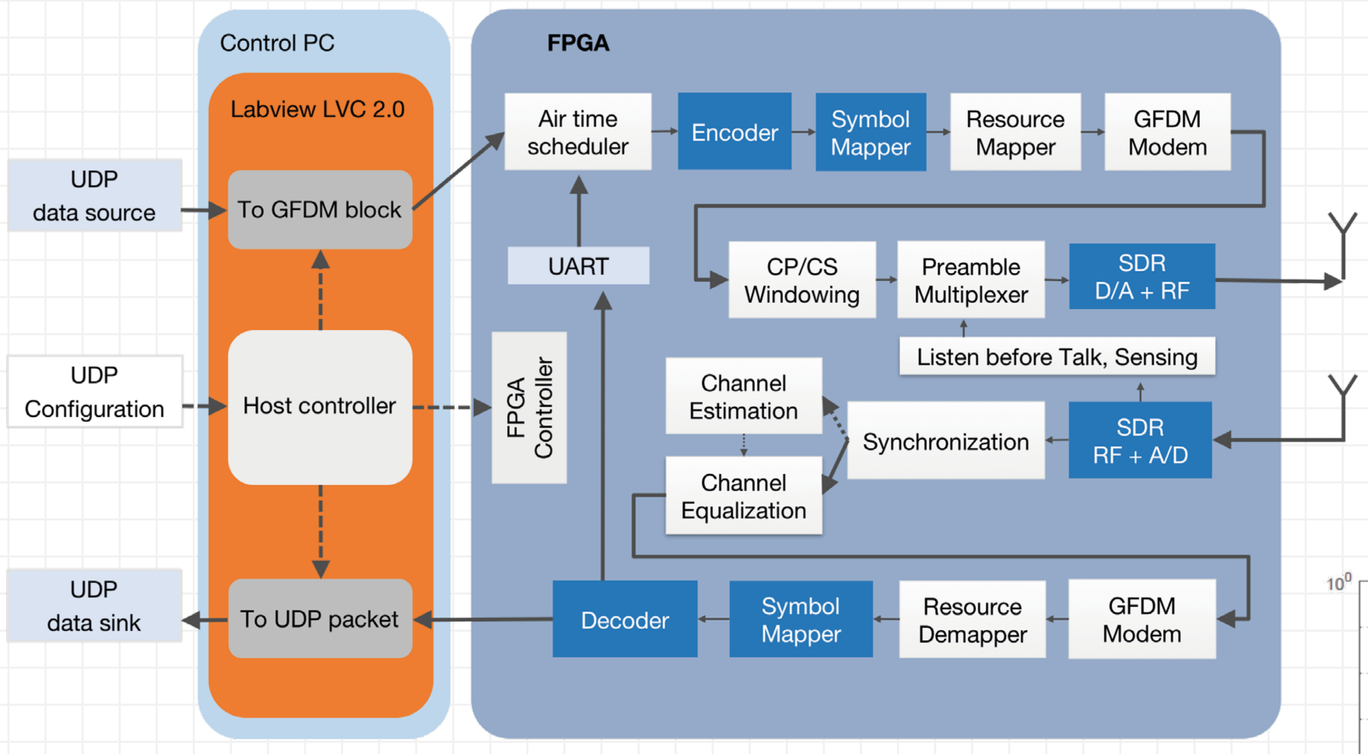
- Configurable RF frond end (FMCOMMS2)
- Zynq 7000 SoC composed by Programmable Logic (running IEEE 802.15.4 compliant transceiver) and Processing system (running MAC on TAISC platform).

ORCA solution 1 offers:

- Better latency performance than commercial chip CC2538
- Tunable latency achieved by changing the signal bandwidth.

	CC2538 (commercial chip)	ORCA Solution 1		
		Narrower Bandwidth	Standard	Wider Bandwidth
Data Rate (Kbps)	250	187.5	250	500
Signal Bandwidth (MHz)	2	1.5	2	4
RTT (PHY level) (ms with 28 bytes in the air)	2.44	2.69	2.049	1.09

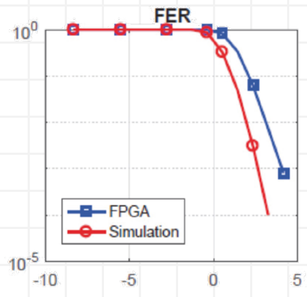
SDR SOLUTION 2: FLEXIBLE PHY BASED ON GFDM

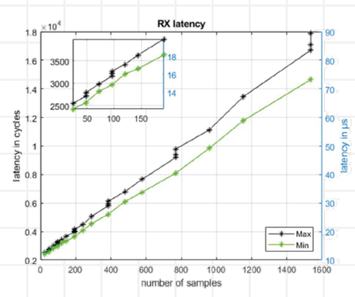


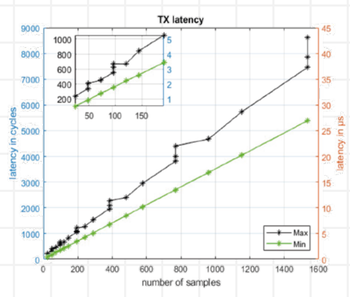
This general overview of the architecture consists of two different parts. All the timing critical signal processing are placed on the FPGA. This includes all the PHY functionalities as well as lower MAC functions such as Listen Before Talk. Higher layer functionality such as MAC, including creation of the headers are executed on a host computer to allow a fully flexible implementation.

ORCA solution 2 offers:

- 200 MHz clock speed (~ 50 MS/s data rate, ~100 MS/s planned, ~200 MS/s possible)
- 9 Bytes Payload (Round-Trip without MAC 100 µs @ 30 MHz BW, First MAC experiments show round-trip latency of around 1.5 ms @ 10 MHz BW)







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