

GRANT



AGREEMENT NO.: 732174

Call: H2020-ICT-2016-2017

Topic: ICT-13-2016

Type of action: RIA



Orchestration and Reconfiguration Control Architecture

D7.2: Summary of results of first Open Call for extensions

Revision: v.1.0

Work package	WP 7
Task	Task 7.2
Due date	31/12/2018
Submission date	21/12/2018
Deliverable lead	IMEC
Version	1.0
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Abstract	D7.2 collects the summaries and conclusions of the first Open Call for Extensions. It introduces the organization of the Call, the winners, and overview of each extension, including its
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	implementation and usage. the main challenges. This deliverable will be used for promotion of the ORCA facility in WP8.
Keywords	Open Call, testbed, SDR, extensions.

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EXECUTIVE SUMMARY

This deliverable reports the work done in the 1st Open Call for Extensions of ORCA project. In this Open Call, 4 distinctive topics are defined. Each of the topics has clearly defined functional and technical requirements, as well as a validation scenario on the ORCA facility. This call is organized in such a way that first the potential candidates submit their proposals to receive feasibility and relevance feedback from patrons, and then a final proposal is prepared based on the feedback. The final proposals are then forwarded to independent external evaluators for evaluation. The winning proposals are selected based on the scores of the evaluation or consensus meeting if differences exist among the external evaluators. After introducing the Open Call's organization, the main targets and results of each of the extensions are introduced. The first extension is developed to support the experimenter in creating and operating in a hybrid SDN-SDR environment for slice experimentation. The second extension consists in designing an IP core running on FPGA of SDR devices, that completes Listen Before Talk functionalities in the spirit of the 3GPP LAA framework. The third extension is developed to realize the LTE-WLAN Radio Aggregation (LWA) and LTE-WLAN Radio Level Integration (LWIP) protocols in NS-3 and their interfacing to ORCA SDR platforms. The last extension is developed to provide ORCA with the desired real-time digital self-interference cancellation (SIC) functionality to the full-duplex platform.

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ABBREVIATIONS

EXT	Extensions
LBT	Listen Before Talk
OC	Open Call
OC1 EXP	First Open Call for Experiments
SDR	Software Defined Radio
SDN	Software Defined Networking

1 INTRODUCTION

The Deliverable 7.2 aims to provide an overview of the results, key outcomes and findings from the First Open Call for Extensions (OC1 EXT).

It will include an overview of the OC1 for Extension, including call information and the winners of the extensions (Chapter 2), and the lessons we learned during the Call's organization. In Chapter 3 an overview is given for each Extension, in terms of the extension's objective, main challenges, results, conclusions and feedback towards the ORCA consortium. Finally we conclude the deliverable.

2 FIRST OPEN CALL FOR EXTENSIONS

2.1 Call Information

The OC1 EXT aims to attract external partners with dedicated expertise to develop functionalities for the ORCA facility.

The following Table 1 demonstrates basic Call information

Project full name	ORCA - Orchestration and Reconfiguration Control Architecture
Project grant agreement No.	732174
Call identifier	ORCA-OC1-EXT
Call title	First ORCA Open Call for Extensions
Submission deadline	Wednesday the 15th November 2017, at 17:00 Brussels local time
Feasibility & relevance check deadline	Wednesday the 8th November 2017, at 17:00 Brussels local time

Table 1 : ORCA OC1 EXT Basic Call Information

The extension topics in OC1 EXT include:

- EXT1 - End-to-end slicing support for SDR and SDN
- EXT2 - LBT functionality on FPGA as an IP core
- EXT3 - RAT interworking on NS-3 based SDR Prototyping Platform
- EXT4 - Digital self-interference cancellation for in-Band Full Duplex

The patrons of the 4 extensions are TCD, IMEC, NI, KUL, respectively

In terms of financial information, the total budget for OC1 EXT: 300,000€. Maximum budget per Extension: 80,000€. It is defined that each project will have guaranteed support of 18,000€, with an extra budget of typically €4500 per Extension will be allocated to the ORCA consortium partner acting as Patron for guaranteed support.

2.2 Winners

An established, independent and impartial evaluation process, of confidential nature has been applied to filter and select the winning proposals. A brief summary of the process is as follows:

- Feasibility and relevance check
 - Candidates provide a first submission
 - Patrons evaluate the feasibility and relevance of the proposals and provide feedback
- Final submission and evaluation
 - Based on the feedback, the proposals passed the feasibility check will submit the final applications
 - External evaluators receive and review the final applications based on a set of criteria and give scores

- Consensus meetings between evaluators were held when necessary to agree on the winners

The following projects have won the ORCA OC1 EXT:

- **EXT1: FINS** (Federating Interface for Network Slicing). Submitted by: FBK CREATE-NET (Italy)
- **EXT2: DOLPHIN** (Detect and avoid LBT Prototyping using Hardware generic design). Submitted by: CEA-Leti (France)
- **EXT3: UP-ORCA** (Unified Platform for Benchmarking 3GPP Unlicensed LTE Flavors in ORCA). Submitted by: Universitat Oberta de Catalunya (Spain)
- **EXT4: Real-Time Digital Self-Interference Canceller for In-band Full-Duplex Enabling up to 100 dB of Total Isolation**. Submitted by: Tampere University of Technology (Finland).

2.3 Observations / Lessons Learned

The consortium, through the organisation process of the OC1 EXT, has the following observations that would like to take into consideration for future OC EXTs:

1. Interface specifications could be included in the call document. During the early implementation phase of the 2nd EXT, we had extensive discussions regarding interface design of this FPGA IP core. This could have been avoided if it is already specified in the call document. Of course a downside is that the 3rd party would have less freedom to do their design.
2. We should try to avoid having a call launched nearby holiday period, as this increases the difficulty to find qualified evaluators.
3. The future OC-EXTs should include support from the OC partners after the delivery of their extension. This suggestion brings two benefits: it decreases the burden to the OC partner of preparing a comprehensive user guide during the period of the extension (so the partners can put more effort on the development of the extension itself), and it facilitates the use of the extension by future OC-EXPs and the ORCA partners (as the developers of the extension can provide a better and faster feedback than the patrons).

3 SUMMARY OF RESULTS IN EACH PROJECT

3.1 EXT1

3.1.1 Goal of this extension

The FINS Framework main purpose is to support the experimenter in creating and operating in a hybrid SDN-SDR environment for slice experimentation. FINS Framework was specifically designed for being used in a remote virtualized testbed, providing support for automating the creation and management different radio-network end-to-end slices, and related resources.

3.1.2 Main challenges

The main challenges in the definition of the FINS Framework were to provide an easy to use user environment (abstracting the slice creation details), to define tools for managing the SDR and SDN available resources, maintaining at the same time the programmability and flexibility of the experiment set-up and to keep it open to future extensions.

3.1.3 Description of concept of extension

FINS framework creates on an IRIS provisioned set of resources an environment capable of processing User requests for the creation of E2E slices over a given topology created with a subset of the available resources. Specific modules are envisioned to interface and control the different types of data-plane resources, according to the instructions coming from a centralized main module.

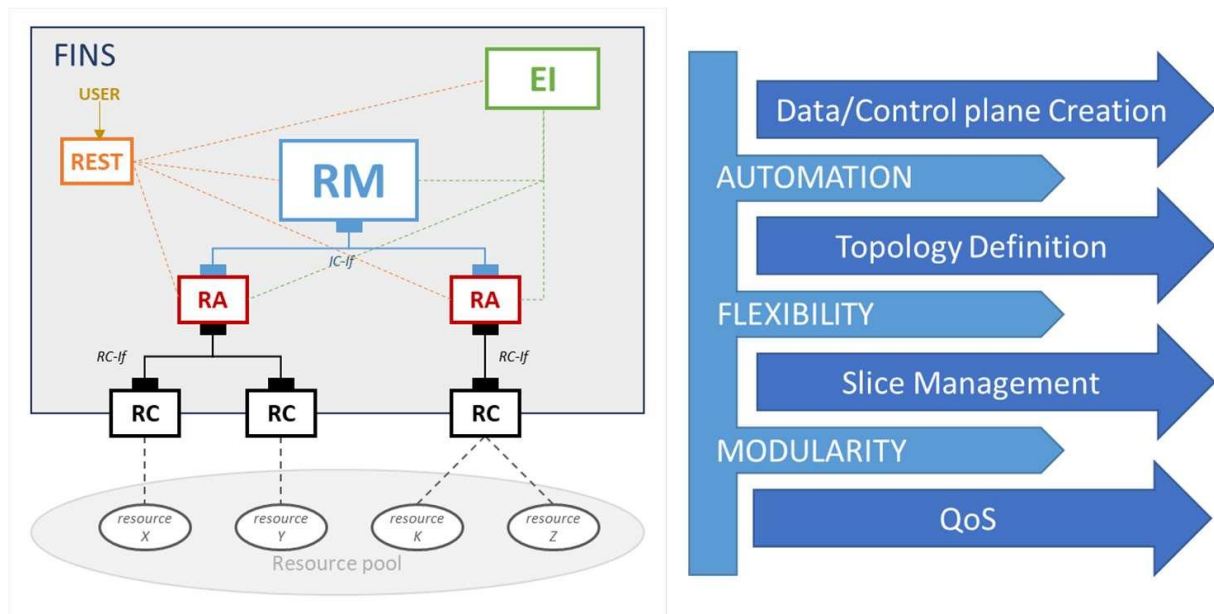


Figure 1 Main concept of EXT1.

3.1.4 Main results

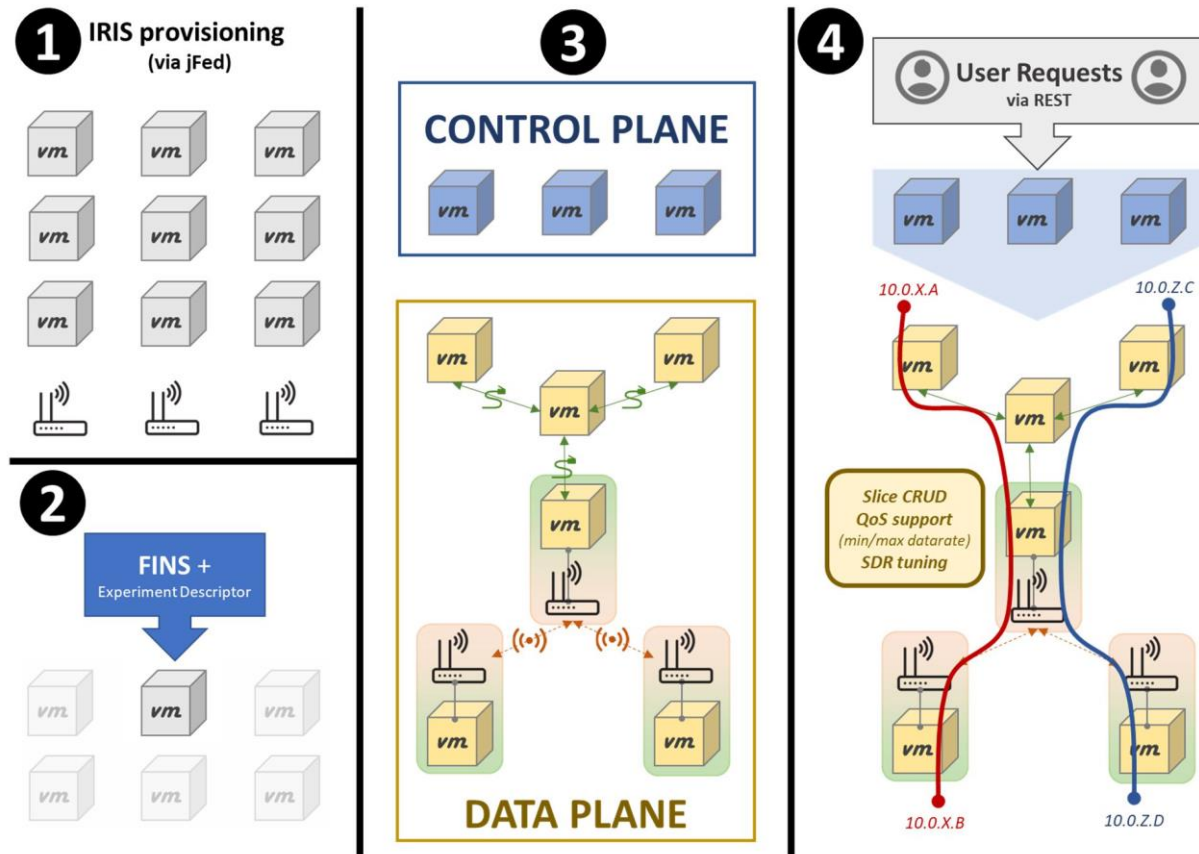


Figure 2 1) Resources (VMs + USRPs) are provisioned by IRIS via jFed; 2) FINS is installed on one of the provisioned machine and run with an experiment descriptor; 3) According to the descriptor, FINS instantiates control- and data-plane, with a given topology created by defining gre tunnels and bridging SDN and SDR components; 4) Control plane receives requests from Experimenter through REST interface and configures and manages Slices, assigns and modifies QoS settings and USRPs' configurations

FINS is an end-to-end SDR/SDN slicing enabling framework for IRIS testbed. After a set of VMs and resources have been provisioned, FINS can be installed on one of those VMs. It requires an experiment configuration file as parameter at launch, to separate the VMs between control- and data-plane and to perform the following operations:

- at control-plane side: instantiation of all the modules required (Experiment Initialiser, Resource Manager, Resource Agents – OVS RA and SDR Controller RA) plus the REST interface and activation of those services that are needed by FINS functioning (mainly, RabbitMQ server)
- at data-plane side: setup and configuration of the OVS bridges and USRPs, plus creation of the GRE tunnels, which are used as links of the imposed topology, and of the tap interfaces required for interconnecting the SDR with SDN components

After completing such operations, FINS is ready for receiving User requests through the REST interface for:

- creating, updating and deleting slices (spanning over SDN, SDR or both)

- assigning specific restrictions over minimum/maximum data-rate over the whole slice or on specific sections. If bandwidth restrictions over different slices are not saturating the capability of the crossed links, created slices are isolated and not interfering with each other.
- modifying the configuration of one or more of the USRPs (in terms of frequency and/or modulation).

3.1.5 Conclusions

In IRIS testbed, FINS framework (through an automated and modular approach) can successfully manage a set of provisioned VMs with associated SDN/SDR resources, by imposing a user-defined topology and instantiating a control plane managing user requests for end-to-end SDR-SDN slices creation, update and deletion, with basic QoS support,

3.1.6 Feedback

ORCA facility (specifically, IRIS testbed) provided a valuable support to the test and development of the FINS solution. With improved robustness and the introduction of some essential tools for a better user experience, it could become a very attractive service for experimenters in the SDR field.

3.2 EXT2

3.2.1 Goal of this extension

The goal of ORCA/DOLPHIN extension consists in designing an IP that completes Listen Before Talk functionalities in the spirit of the 3GPP LAA framework. It is able to simultaneously monitor up to 8 channels of 20 MHz bandwidth. Based on sensing information, the module establishes communication on selected channels. It is also able to deal with 4 pre-load PHY layer.

The second step of the project is to integrate the IP into two platforms on the ORCA testbed and to carry out “on-air” measurements that emphasize the impact of the secondary LBT system transmission on primary system such as WiFi.

3.2.2 Main challenges

The main challenge of ORCA/DOLPHIN is to have a first hardware step in multi-channel LBT algorithm that enables to investigate the perturbation on others systems. For that purpose, it is able to compute some statistic variables to characterize the secondary emission activity, and the sensing sensitivity.

The design genericity is also one of the key point. The LBT IP has been remotely integrated on prototyping Xilinx board (ZC706) and RF-NOC based board (Ettus X310) that are part of the IMEC testbed.

3.2.3 Description of concept of extension

The setup of the main experiment consists in aggressor / victim scenario. The Aggressor will be the LBT system where as the victim will be an existing system such as WiFi.

The LBT module is based on periodic sensing to yield emission (or not) of a pre-loaded frame.

The LBT module has to show the ability of changing channel or measure the impact on WiFi when secondary emission occurs in the same channel.

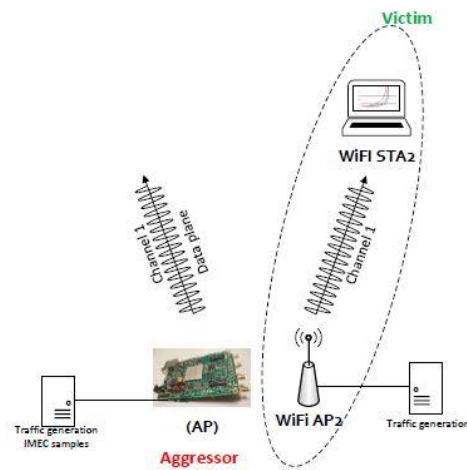


Figure 3 Main concept of EXT2

3.2.4 Main results

The following figure shows respectively the timing of the periodic sensing that has been implemented in the LBT state machine and the impact of LBT module on WiFi. The WiFi acts as primary system, formed by two commercial IEEE 802.11g compliant nodes. There are 3 main cases:

- Small sensing period: The impact on WiFi is maximum, the system occupies the channel most of the time (>98% of the time).
- Sensing period close to secondary frame length duration: the channel occupancy of the secondary emission is 70% and the WiFi throughput falls to 22Mbps (max = 27Mbps).
- Long sensing period (>> secondary frame duration): In this zone, the impact on WiFi can be mitigated according to the targeted throughput loss.

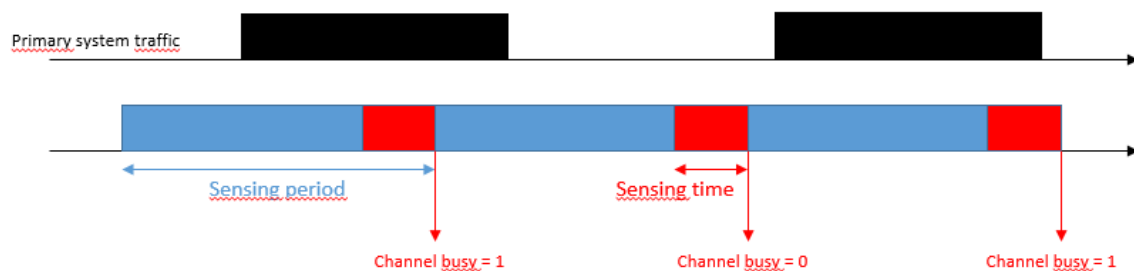


Figure 4 LBT sensing period vs primary traffic

Full curves are related to channel occupancy when the LBT system transmits whatever the sensed power is. The dotted curve shows the impact on WiFi characterized by its throughput. “High threshold” is set to get a secondary emission at each opportunity (i.e. at the end of the sensing period) whatever the primary system power is. “Low threshold” is set to get a secondary emission based on the sensing status.

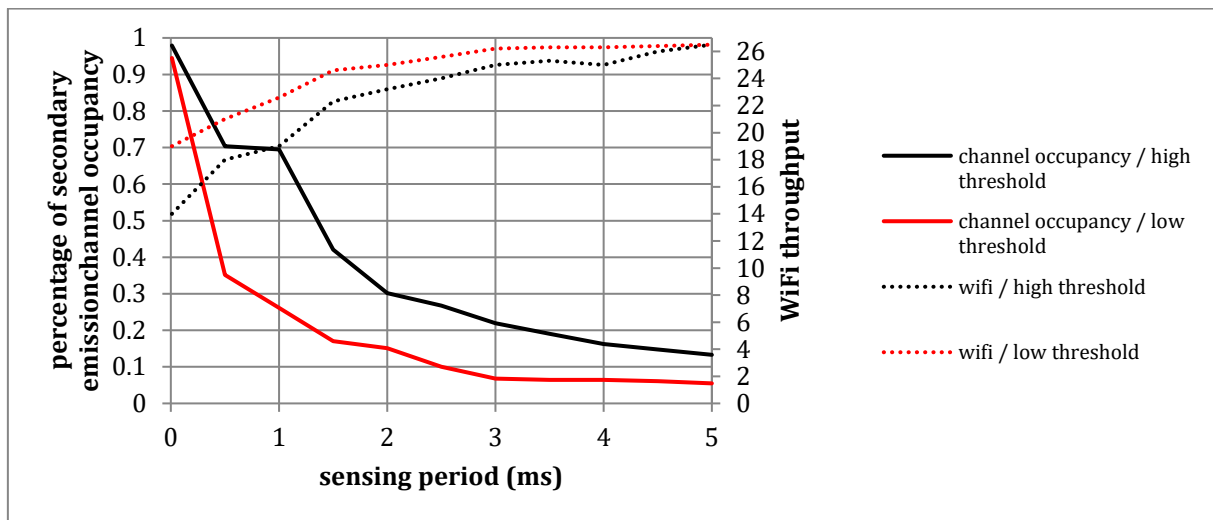


Figure 5 EXT2 main results, impact on of LTE emission controlled by LBT core on Wi-Fi traffic

3.2.5 Conclusions

The proposed extension consists in designing a generic and configurable multi-channel Listen Before Talk (LBT) processor able to monitor a number of radio channels and trigger the emission of data streams over-the-air. The IP includes specific and classic in/out interfaces, that enables the integration in several hardware environments: basic AD/DA convertors interface and AXI-stream interfaces that enable on the one hand to access the IP via Direct Memory Access process and on the other hand connection with RF-NOC architecture. The chosen platform emphasises the agility of the design to face different kind of hardware components and different integration techniques.

The IP has been remotely integrated on the IMEC testbed, and tests have been run to validate each of all core IP functionalities. Then, based on an approach along the 3GPP LAA validation test, an “aggressor” (secondary transmission from LBT) vs “victim” (WiFi) scenario has been run. Measurement campaign shows that a periodic sensing can deal with a WiFi transmission and that the impact on WiFi (throughput) can be mitigated according to the sensing period.

3.2.6 Feedback

Excellent communication with the patron and ability to access and provide an additional feature to a versatile and open platform.

3.3 EXT3

3.3.1 Goal of this extension

We present the implementation of the LTE-WLAN Radio Aggregation (LWA) and LTE-WLAN Radio Level Integration (LWIP) protocols in NS-3 and their interfacing to ORCA SDR platforms. This implementation has been used to compare both technologies under different network conditions. It can also enable researchers and practitioners to explore online protocol orchestration depending on LTE and WiFi network status.

3.3.2 Main challenges

In this extension we have approached two main challenges. The first one has been the implementation of LWA and LWIP in NS-3 which has required enabling communication among devices belonging to different technologies and extracting packets at different layers of the protocol stack. The second one

has been the interfacing to SDR platforms which has been possible thanks to the NI L1-L2 APIs development and the TU Dresden Testbed.

3.3.3 Description of concept of extension

Our implementation of LWA and LWIP has been interfaced to the ORCA SDR platforms using the NI L1-L2 APIs. We have implemented the LTE eNB, WiFi AP, LTE UE and WiFi STA running in 4 SDR devices and provide this testbed setup for future experimenters in the TU Dresden Testbed. Interfacing to other platforms (such as srsLTE or/and open WiFi SDR platforms) can be achieved without modifications in the provided NS-3 code and by developing the required APIs. This development can be done with the help of the NI L1-L2 API development description provided by NI.

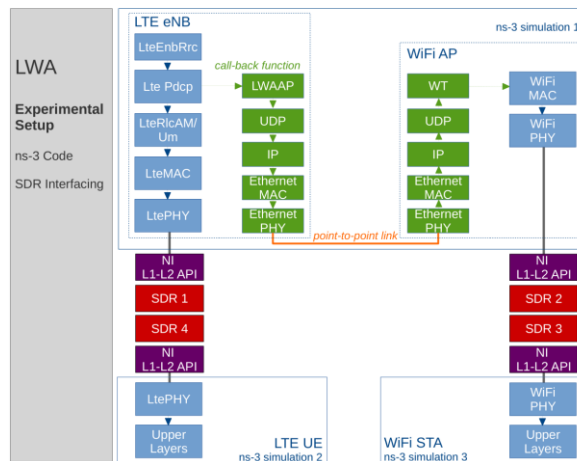


Figure 6: Block diagram of LWA implementation.

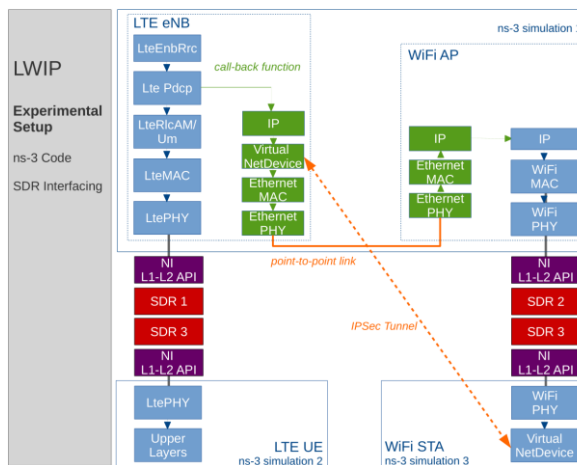


Figure 7: Block diagram of LWIP implementation.

3.3.4 Main results

We have evaluated LWA and LWIP in NS-3 with the goal to obtain more insight on their ability to augment LTE channel capacity under different settings and network conditions. We have seen that LWIP is slightly more inefficient due to the need to include IPSec overhead in the packet headers, which reduce the effective data that can be transmitted per channel attempt. This effect has more impact when the packets to be transmitted are small and persist when moderate contention with coexisting WiFi networks is considered. We have also evaluated the effect of having interferer WiFi networks in the vicinity and how the impact on throughput varies by changing the distance and transmission power.

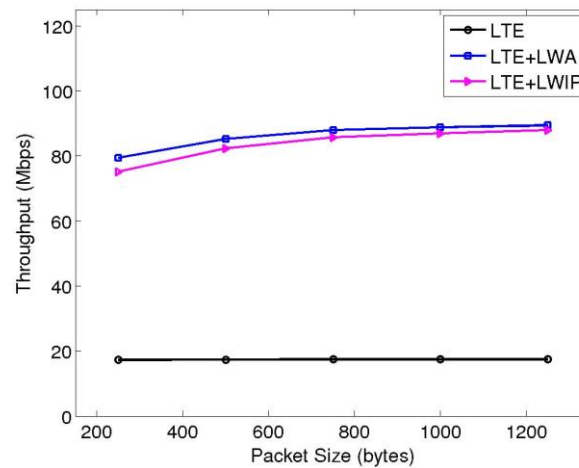


Figure 8: Performance of LWA and LWIP without interference.

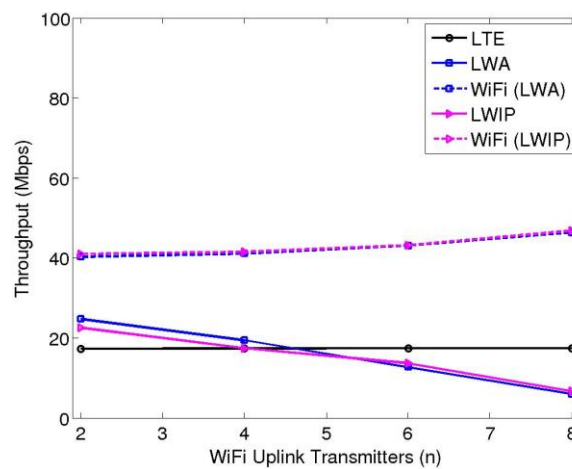


Figure 9: Performance of LWA and LWIP with interference.

3.3.5 Conclusions

This extension has allowed us to obtain a first take on which technology is more suitable to use depending on the network conditions. We have compared how effectively both technologies augment LTE capacity with varying packet sizes and at different conditions of interference with WiFi. This extension also enables researchers and practitioners to further evaluate both approaches and devise ways forward to protocol orchestration.

3.3.6 Feedback

Our experience with the TU Dresden Testbed as well as the communication with the Patron have been satisfactory. We also value highly the resources and experience we have gained in this extension, especially the Patron background on SDR interfacing as well as their L1-L2 APIs. We also value the research outcomes from this extension, which enable new research directions on online LWA /LWIP protocol orchestration.

3.4 EXT4

3.4.1 Goal of this extension

The main objective of this Extension was to provide ORCA with the desired real-time digital self-interference cancellation (SIC) functionality to the full-duplex platform, which would fulfil the following functional and technical requirement, as stated in the call:

- 45-50 dB of digital self-interference cancellation
- implementation on the field-programmable gate array (FPGA) on the current ORCA IBFD platform
- provide flexibility in terms of implementation platform
- support for IEEE 802.15.4 and IEEE 802.11p waveforms.

In addition to meeting these requirements, the wider scientific objective was to develop a high performance and resource-efficient nonlinear digital SIC solution, which, as part of the ORCA IBFD platform, would have high impact in terms of advancing IBFD experimental research and industrial adoption.

3.4.2 Main challenges

The real-time implementation of the system with a reasonable resource consumption was a critical challenge in this work. To overcome this challenge, we implemented the digital canceller both by LabVIEW FPGA and Catapult HLS. Since the FPGA code of the ORCA testbed is originally implemented by LabVIEW, we achieved better results using LabVIEW communication software.

3.4.3 Description of concept of extension

Figure 10 shows a high-level block diagram of the considered IBFD transceiver on a software defined radio (SDR) platform, and the developed digital SIC solution implemented on the FPGA. The transmitter (TX) and receiver (RX) share the same antenna, being connected through an electrical balance duplexer (EBD) to provide RF isolation/cancellation. The EBD gives TX-RX isolation of about 50 dB, which is sufficient to protect the receiver in most practical cases. The signal then goes through the receiver RF front-end and analog-to-digital conversion (ADC), after which the digital cancellation signal, which is an internally generated replica of the self-interference, is subtracted from the received signal. After the subtraction, the received signal is used together with the original transmit data to update the coefficients of the digital SIC. The concept involved the development of a novel, resource-efficient, DSIC algorithm, its real-time implementation to VHDL with HLS approach, and the integration of this block into the ORCA full-duplex LabVIEW platform. An alternative FPGA implementation of the algorithm using LabVIEW FPGA tools was also developed in parallel, in order to have a proper reference model.

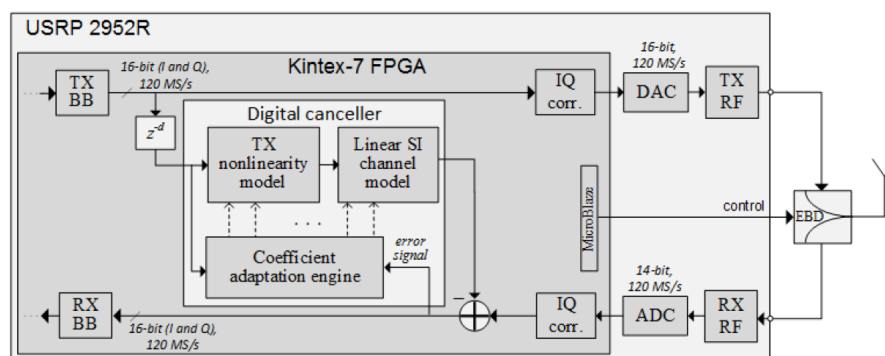


Figure 10. High-level block diagram of the considered IBFD transceiver on the SDR platform, focusing on the developed digital SIC solution on the FPGA.

3.4.4 Main results

First, the functionality of the canceller is validated by turning the transmission on in the device the EBD is attached to. Without tuning the EBD, the transmitted signal is attenuated only slightly (20-25 dB) due to the intrinsic isolation of the EBD. The received signal is then cancelled using the developed digital self-interference canceller. The power spectral densities of the measured signal without and with digital cancellation are shown in Figure 11. The calculated in-band cancellation of the canceller is 47.2 dB in this case, thus showing that beyond 45 dBs of digital cancellation can be achieved. Next, the functionality is tested in conjunction with the EBD. This time, after the transmission starts, the EBD is tuned and it offers some cancellation of the signal. Then the self-interference canceller is turned on. In Figure 12, all the corresponding spectral densities are presented, corresponding to:

- EBD, no tuning: Spectra of the leakage signal coming from the TX chain. This is the signal the EBD and the canceller aims at suppressing.
- EBD, tuned: RF cancellation with the duplexer. Tuning the EBD provides 30 dB of cancellation compared to the untuned case.
- EBD, tuned + DSIC: RF + digital cancellation. The LabVIEW digital canceller implementation provides a further cancellation of 30 dB in this particular example case. After the last stage of

the cancellation process, the power density of the error signal remains at approximately -50 dB, less than 10 dB above the noise floor level.

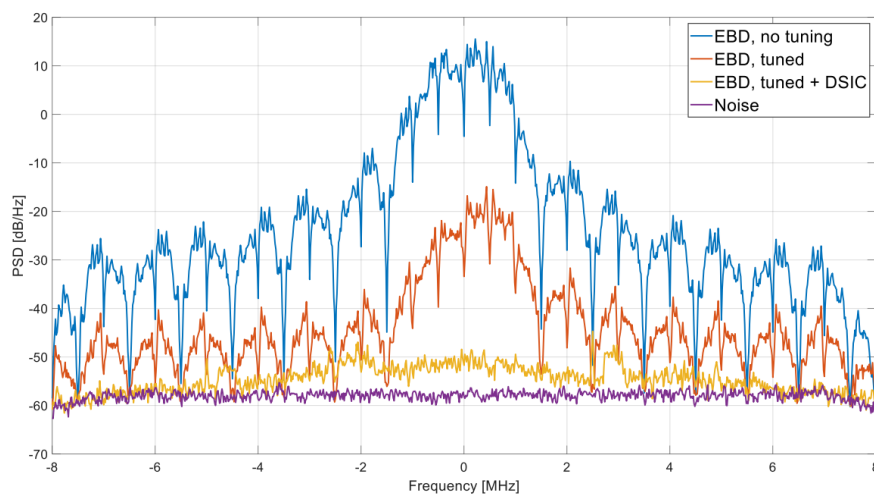


Figure 11. Power spectral density of the signal without and with digital self-interference cancellation

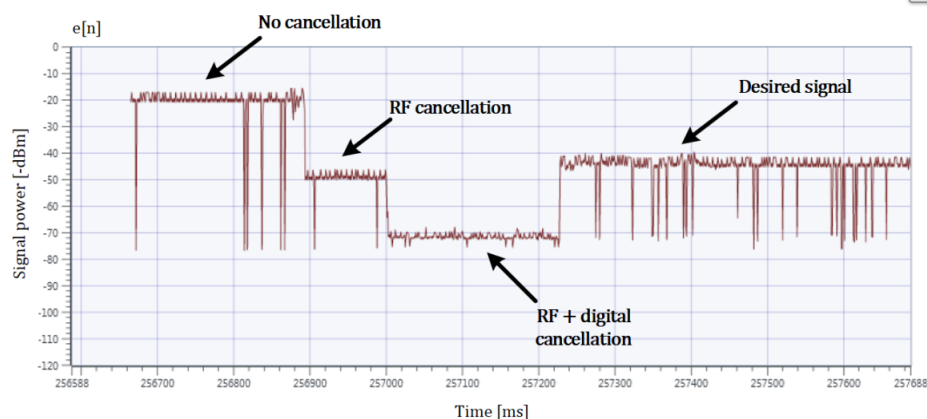


Figure 12. Error signal power in the considered scenario.

3.4.5 Conclusions

This extension provided the ORCA full-duplex testbed the required real-time DSIC capability. The DSIC implementation greatly facilitates the operation of the ORCA full-duplex testbed, since without it, the functionality in terms of transmit power and range would be extremely limited. With the DSIC in place, real-time PHY and MAC layer operation with actual full-duplexing are possible on the testbed, as one of the first testbeds in the world. The ORCA partners and collaborators will thus have access to a cutting-edge experimental testbed with state-of-the-art performance. This extension will thus facilitate and further research efforts on future full-duplex technology within the EU as well as globally.

3.4.6 Feedback

ORCA gave us the opportunity to continue working on digital self-interference cancellation technology, develop a new DSIC algorithm, and implement it on FPGA. The implementation expands our possibilities at TUT to do experimental full-duplex research in the future. Thanks to ORCA, we have established a good collaboration with the Patron (KUL), and this collaboration will hopefully continue also after this project. Communication and cooperation with the Patron also was very good, and especially the help and advice on LabVIEW that we got from the Patron proved crucial for the success of the project.

4 CONCLUSIONS

This deliverable reports on the work done during the 1st Open Call for Extensions of the ORCA project. First the organizations of the Call is introduced, and then the results of each extension topics are given. In this Open Call, 4 distinctive topics are defined, as listed below.

- EXT1 - End-to-end slicing support for SDR and SDN
- EXT2 - LBT functionality on FPGA as an IP core
- EXT3 - RAT interworking on NS-3 based SDR Prototyping Platform
- EXT4 - Digital self-interference cancellation for in-Band Full Duplex

The winning proposals are selected by scores given by independent external evaluators. The extensions are then implemented by qualified 3rd parties, and validated on at least one ORCA facility. All the third parties have met the technical and functional requirements specified in this call.